EXHIBIT 18

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
OAKLAND DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC and MCM PORTFOLIO LLC, Plaintiffs, v. CANON INC., et al., Defendants.	Civil Action No. 14-03640 CW DECLARATION OF DR. GARY S. TJADEN IN RESPONSE TO THE AUGUST 12, 2012 DECLARATION OF DALE E. BUSCAINO
TECHNOLOGY PROPERTIES LIMITED LLC and MCM PORTFOLIO LLC, Plaintiffs, v. FALCON NORTHWEST COMPUTER SYSTEMS, INC., Defendant.	Civil Action No. 14-03641 CW DECLARATION OF DR. GARY S. TJADEN IN RESPONSE TO THE AUGUST 12, 2012 DECLARATION OF DALE E. BUSCAINO
TECHNOLOGY PROPERTIES LIMITED LLC and MCM PORTFOLIO LLC, Plaintiffs, v. HEWLETT-PACKARD COMPANY, Defendant.	Civil Action No. 14-03643 CW DECLARATION OF DR. GARY S. TJADEN IN RESPONSE TO THE AUGUST 12, 2012 DECLARATION OF DALE E. BUSCAINO
TECHNOLOGY PROPERTIES LIMITED LLC and MCM PORTFOLIO LLC, Plaintiffs, v. NEWEGG INC., et al., Defendants.	Civil Action No. 14-03645 CW DECLARATION OF DR. GARY S. TJADEN IN RESPONSE TO THE AUGUST 12, 2012 DECLARATION OF DALE E. BUSCAINO

TECHNOLOGY PROPERTIES LIMITED LLC and MCM PORTFOLIO LLC, Plaintiffs, v. SEIKO EPSON CORPORATION., et al., Defendants.	Civil Action No. 14-03646 CW DECLARATION OF DR. GARY S. TJADEN IN RESPONSE TO THE AUGUST 12, 2012 DECLARATION OF DALE E. BUSCAINO

DECLARATION OF DR. GARY S. TJADEN IN RESPONSE TO THE AUGUST 2, 2012 DECLARATION OF DALE E. BUSCAINO SUBMITTED BY PLAINTIFFS IN SUPPORT OF THEIR OPENING CLAIM CONSTRUCTION BRIEF

I, Gary S. Tjaden, declare as follows:

1. My name is Gary S. Tjaden. I currently reside at 135 Compass Point Drive, Saint Simons Island, Georgia 31522.

I. BACKGROUND

2. I have been retained as an expert witness in this litigation by defendants Canon Inc.; Canon U.S.A., Inc.; Hewlett-Packard Company; Newegg Inc.; Rosewill Inc.; Seiko Epson Corporation; Epson America, Inc.; and Falcon Northwest Computer Systems, Inc. (collectively, "Defendants"). I was asked to respond to certain statements in the August 2, 2012 Declaration of Dale E. Buscaino filed in support of TPL's Opening Claim Construction Brief ("the Buscaino 2012 Declaration").

3. My detailed educational and professional background and a list of my technical publications for the preceding 46 years are described in my curriculum vitae, attached hereto as EXHIBIT 1. My curriculum vitae also lists the cases in which I have testified as an expert at trial or by deposition.

4. I am the Founder and am currently President of COCOMO ID, LLC, a developer of technology for mobilized text-audio publishing.

5. From 1993 through 2004, I was a Principal Research Engineer and Director of the Center for Enterprise Systems at the Georgia Institute of Technology. Before coming to the Georgia Institute of Technology, I held numerous executive positions with NYNEX Corporation (1987-92), a regional telecommunication service provider, and with Burroughs/Unisys (1984-87), a manufacturer of computer systems and provider of information technology services. I also was Senior Vice President of Engineering and Technology for Cox Cable Communications from 1979 to 1984, where I was involved in various company activities and ventures, including supervising development and implementation of the company's interactive cable-based videotext system known as INDAX. Prior to joining Cox, I held research and development posts with Sperry

Corporation in both the Sperry Research Center located in Sudbury, Massachusetts (1975-76) and the Univac Division located in Bluebell, Pennsylvania (1976-79), and with the Bell Telephone Laboratories Electronic Switching Systems Division located in Naperville, Illinois (1966-70 and 1972-75).

6. During my employment at the Bell Telephone Laboratories, I served as a Member of the Technical Staff involved with the design and development of electronic circuits, including integrated circuits, related to peripheral components of multiple versions of electronic switching systems. I designed and developed printed circuit boards, including the physical connectors and housings. This particular experience is directly relevant to the issues about which I have been asked to opine in this Declaration.

7. I am a named inventor of eight issued U.S. patents.

8. I hold a Bachelor of Science degree in Electrical Engineering (B.S.E.E.), which I received from the University of Utah in 1966. I received a Master of Science degree in Electrical Engineering (M.S.E.E.) in 1969 from Northwestern University. In 1973, I received a Doctor of Philosophy (Ph.D.) degree in Computer Science from The Johns Hopkins University.

9. In forming my opinions, I have reviewed the following information: TPL's Opening Claim Construction Brief and exhibits in this litigation, including the Buscaino 2012 Declaration; U.S. Patent No. 7,295,443; U.S. Patent No. 7,522,424; and U.S. Patent No. 7,719,847 (collectively "the Patents"); the file histories for the Patents; U.S. Patent No. 6,438,638; and U.S. Patent No. 6,402,558 to Hung-Ju et al. cited during the prosecution of the '443 patent.

10. I understand that the Court has not yet determined what the qualifications of a person of ordinary skill in the art would have been with respect to the Patents. Based on my experience, I believe the level of ordinary skill in the relevant art for the Patents would best be defined as a combination of education and experience. For example, I would consider an engineer with a bachelor of science degree in electrical engineering and two to four years of experience in electronic circuit design, packaging, and software engineering to possess an ordinary level of skill in the field of endeavor of the Patents. The more formal education one has,

the less industry experience needed to attain an ordinary level of skill. I believe I am a person of at least ordinary skill in the art related to the Patents.

11. I understand from counsel that determining the proper construction for claim terms is a legal issue for the Court to decide, and I further understand that the purpose of claim construction is to determine how one skilled in the art would have understood the claim terms at the time of the alleged invention.

II. STRUCTURE CORRESPONDING TO "MEANS FOR MAPPING"

12. I understand from counsel that certain terms in patent claims may be expressed in "means plus function" language and subject to the requirements of 35 U.S.C § 112, ¶6, which provides that such claim limitation "be construed to cover the corresponding structure . . . described in the specification and the equivalents thereof." I further understand from counsel that the corresponding structure in the specification is "corresponding structure" only if the specification or the prosecution history clearly links or associates that structure to the claimed function.

13. I further understand from counsel that, where the function of a "means-plus-function" term is performed by a general purpose computer or microprocessor, the "structure" to be identified in the specification includes not only the computer itself but also an algorithm by which the computer performs the claimed function. And I understand that such algorithm must be disclosed in the patent's specification, and that a patentee cannot rely on the knowledge of one skilled in the art to fill in the gaps for corresponding structure.

14. I understand that the parties do not dispute that each of the following terms is governed by 35 U.S.C. § 112, ¶ 6 and thus these terms are "means plus function" terms:

'424 patent, claim 25: (i) means for mapping power, ground or data signals between said interconnection pins and said one or more contact pins depending upon the identification of the type of memory card inserted into said port;

'424 patent, claim 28: (ii) means for mapping power, ground or data signals between said interconnection means and said one or more contact pins depending upon the identification of the type of memory card inserted into said port; and

'847 patent; claim 1: (iii) means for mapping power, ground or data signals between said signal lines and said one or more contact pins depending upon the identification of the type of memory card inserted into said port.

15. I understand that TPL offered the Buscaino 2012 Declaration in support of its proposed construction with respect to these three "means for mapping" terms identified in ¶ 14. Mr. Buscaino's opinions with respect to the construction of these terms are set forth in ¶¶ 16-31 of the Buscaino 2012 Declaration. Accordingly, in the following paragraphs of this Declaration, I respond to specific paragraphs of the Buscaino 2012 Declaration.

16. With respect to ¶ 16 of the Buscaino 2012 Declaration, and as I stated above, I understand that there is dispute between the parties regarding the "means for mapping" terms set forth in paragraph 14 above. I also understand that the Defendants assert that claims 25 and 28 of the '424 patent – and claims 26 and 29 depending therefrom, respectively – and claim 1 of the '847 patent are invalid as indefinite under 35 U.S.C. § 112, ¶2.

17. With respect to ¶ 17 of the Buscaino 2012 Declaration, I disagree with Mr. Buscaino's opinion that one of ordinary skill in the art at the time of the '424, '847 and '638 patents would have understood the "scope" of claims 25 and 28 of the '424 patent and claim 1 of the '847 patent for the reasons described herein. I take no position at this time on the issue of the priority date to which the claims of the '424 and '847 patents are entitled.

18. With respect to ¶ 18 of the Buscaino 2012 Declaration, I understand that Defendants have asserted that there is not sufficient structure disclosed in the specifications of the '424 and '847 patents associated with the function of "mapping power, ground or data signals . . ." in claim 25 of the '424 patent, claim 28 of the '424 patent, and claim 1 of the '847 patent. I understand that one reason Defendants assert that there is not sufficient structure disclosed is because there is no disclosure of an algorithm for performing the function of "mapping power, ground or data signals . . ." in claim 25 of the '424 patent, claim 28 of the '424 patent, and claim 1 of the '847 patent. For the reasons provided herein, I agree with Defendants and therefore disagree with Mr. Buscaino on this issue.

19. With respect to ¶ 19 of the Buscaino 2012 Declaration, based on my own review of the Patents (specification and claims) and the prosecution histories for the Patents, I disagree with Mr. Buscaino's opinion. In my opinion, the specification of the '424 patent does not properly disclose corresponding structure for performing the function of "mapping power, ground or data signals between said interconnection [pins/means] and said one or more contact pins depending upon the identification of the type of memory card inserted into said port." The specification for the '847 patent does not properly disclose corresponding structure for performing the function of "mapping power, ground or data signals between said signal lines and said one or more contact pins depending upon the identification of the type of memory card inserted into said port." Finally, the specification for the '638 patent does not properly disclose corresponding structure for performing the function of "mapping power, ground or data signals between said [interconnection pins/interconnection means/signal lines] and said one or more contact pins depending upon the identification of the type of memory card inserted into said port."

20. With respect to ¶ 20 of the Buscaino 2012 Declaration, the only structure disclosed in the '424 and '847 patent specifications that is potentially capable of performing the mapping functions set forth in claims 25 and 28 of the '424 patent and claim 1 of the '847 patent is a controller or controller chip. Based on my review of the '424 patent and the '847 patent and the prosecution histories for the Patents, neither the '424 patent nor the '847 patent has any disclosure that indicates that the controller or controller chip is a "computer-less, microprocessor-less integrated circuit," as Mr. Buscaino alleges in ¶ 20, or whether the controller may be a computer-based or microprocessor-based integrated circuit as Mr. Buscaino acknowledges in ¶ 21. The '424 patent and '847 patent have no disclosure to identify what structure is used for the controller or controller chip. I note, however, that the '424 and '847 patents both refer to a ROM provided with a controller. Specifically, the Patents provide: "For example, the adapter may be formed of a single piece of molded plastic, with the controller chip and an associated memory device (e.g., ROM) embedded into the molded plastic." *See*, '424 pat., Col. 7:53-56; '847 pat., Col. 7:35-39. In my experience, ROMs (read-only memories) are typically provided with controllers or

controller chips to store program instructions to be executed by the controller or controller chip. Thus, this passage suggests the controller or controller chip disclosed in the specification is a computer-based or microprocessor-based controller or controller chip, contrary to Mr. Buscaino's characterization. Based on experience and my review of the Patents and the prosecution histories for the Patents, I disagree with Mr. Buscaino's opinion that a controller or controller chip disclosed in the Patents without some algorithm or programming would be capable of performing the claimed mapping function.

21. With respect to ¶ 21 of the Buscaino 2012 Declaration, the controller and controller chip disclosed in the '424 patent and the '847 patent require an algorithm or programming to perform the claimed "mapping" functions (see ¶ 14 above). However, I disagree with Mr. Buscaino's opinion that one of ordinary skill in the art would find such an algorithm or programming for performing the claimed "mapping functions" (see ¶ 14 above) in the '424 patent or the '847 patent.

22. With respect to ¶ 22 of the Buscaino 2012 Declaration, I have reviewed the figures (Figs. 4 and 5 of the '424 and '847 patents) and the columns of text from the patents ('424 pat., Col. 5:54-6:63; '847 pat., Col. 5:41-6[7][sic]:49) cited by Mr. Buscaino as purportedly disclosing an algorithm for use with a controller or controller chip for performing the claimed mapping function (¶ 14). I disagree with Mr. Buscaino's opinion that such Figures and lines from the specification disclose a sufficient algorithm for performing the claimed function of mapping.

23. With respect to ¶ 23 of the Buscaino 2012 Declaration, Figures 4 and 5 from the '424 patent each disclose "pin mapping" tables. I disagree with Mr. Buscaino that such tables disclose an algorithm for performing the claimed "mapping functions" (see ¶ 14 above) in the '424 patent or the '847 patent. Figures 4 and 5 from the '424 patent only show the prewired connections of signal lines between multiple sets of contact pins and a discrete set of connector pins – 21 connector pins for Figure 4 and 18 connector pins for Figure 5. These assignments are prewired and fixed before any card is inserted. These contact pin to connector pin connections would include the connection of power, ground and data lines. Nowhere in these "pin mapping" tables is there any disclosure of a step-by-step procedure (i.e., an algorithm) which a controller

would execute to determine the assignment of signal lines to connector pins based upon which type of memory card is inserted into an adapter with a common set of contact pins used for multiple types of memory cards.

24. With respect to ¶ 24 of the Buscaino 2012 Declaration, Figure 4 of the '424 patent includes a column for the Smart Media card. The table in Figure 4 shows that D1-D7 from the Smart Media card column are assigned to connector pins 2 through 8, Ground from the Smart Media card column is assigned to connector pin 18, and Power from the Smart Media card column is assigned to connector pin 19. This is merely one specific instance of fixed assignments for one type of memory card to a set of contact pins for that specific type of card; it is not a disclosure of an algorithm disclosing how signal lines are varied between connector pins and a common set of contact pins used for multiple types of memory cards. These assignments are prewired and fixed before any card is inserted. Therefore, I disagree with Mr. Buscaino's opinion that Figure 4 teaches an algorithm for mapping as claimed in claims 25 and 28 of the '424 patent and in claim 1 of the '847 patent.

25. With respect to ¶ 25 of the Buscaino 2012 Declaration, Figure 5 of the '424 patent includes a column for the xD card. The table in Figure 5 shows that D0-D7 from the xD card column are assigned to connectors pins 10 through 17, Ground from the xD card column is assigned to connector pin 1, and Power from the xD card column is assigned to connector pin 18. Again, as above, this is merely one specific instance of fixed assignments for one type of memory card to a set of contact pins for that specific type of card; it is not a disclosure of an algorithm disclosing how signal lines are varied between connector pins and a common set of contact pins used for multiple types of memory cards. These assignments are prewired and fixed before any card is inserted. Therefore, I disagree with Mr. Buscaino's opinion that Figure 5 teaches an algorithm for mapping as claimed in claims 25 and 28 of the '424 patent and in claim 1 of the '847 patent.

26. With respect to ¶ 26 of the Buscaino 2012 Declaration, I reviewed Figure 5 of the '638 patent and the associated specification disclosure, which is found at the '638 patent, Cols. 7:34-8:20. I disagree with Mr. Buscaino's opinion that Figure 5 of the '638 patent teaches an

algorithm for "mapping" as claimed in claims 25 and 28 of the '424 patent and in claim 1 of the '847 patent. I found no disclosure in the patents that describe any mapping operation between MMC and SD cards. Figure 5 of the '638 patent lists a common set of signals for both card formats in a common "MMC/SD" column. Moreover, I found no disclosure in Figure 5 of the '638 patent, or its associated discussion, that refers to any process that treats MMC cards separately from SD cards. Figure 5 and its associated discussion continuously refer to MMC cards and SD cards using a common term – "MMC/SD". I reviewed the '424 and '847 patents and Figures 4 and 5. I found no disclosure in the patents that describe any mapping operation between MMC and SD cards. Figures 4 and 5 both list common sets of signals for both card formats in a common MMC/SD column. Contrary to the assertions in the Buscaino 2012 Declaration, there is nothing specifically included in the '424 patent, the '847 patent or the '638 patent related to the "4-bit parallel mode" being used by the SD card and not the MMC card.

27. With respect to ¶ 27 of the Buscaino 2012 Declaration, the text cited by Mr. Buscaino from the '424 patent (Col. 5:54-6:57) and the '847 patent (Col. 5:41-6:49) generally describes the use of different types of memory cards and the connection of different sets of contact pins to the connector pins consistent with what is shown in Figures 4 (21 pin connector) and 5 (18 pin connector) in the '424 patent and the '847 patent. Nowhere in these "pin mapping" tables is there any disclosure of a step-by-step procedure (i.e., an algorithm) which a controller would execute to determine the assignment of signal lines to connector pins based upon which type of memory card is inserted into an adapter with a common set of contact pins used for multiple types of memory cards. Therefore, I disagree that this text from the patents teaches an algorithm for "mapping" as claimed in claims 25 and 28 of the '424 patent and in claim 1 of the '847 patent.

28. With respect to ¶ 28 of the Buscaino 2012 Declaration, in both the '424 patent (Col. 6:41-43) and the '847 patent (Col. 6:29-31) only a single specific reference is made to the '638 patent. The passage in the '424 and '847 patent specifications states: "As described in application Ser. No. 09/610,904 (now U.S. Pat. No. 6,438,638), the signal lines to the controller are normally pulled high. When a card is inserted, the card pulls its connected pins low.

Detection of card type is determined by detection of which of the mapped card detect lines is pulled low as illustrated in FIG. 5, or by the (binary) state of data or other card pins mapped to a common set of controller pins as described in the aforesaid parent application. See, e.g., FIGS. 4A-E thereof." Nowhere in these "pin mapping" tables is there any disclosure of a step-by-step procedure (i.e., an algorithm) which a controller would execute to determine the assignment of signal lines to connector pins based upon which type of memory card is inserted into an adapter with a common set of contact pins used for multiple types of memory cards. Rather, the passage refers to the technique disclosed in the '638 patent for detecting the type of memory card inserted into the '638 card adapters. But, this card detection technique does not apply to the '424 and '847 patents, because the '638 patent teaches that the card detect indicators are provided by a unique physical adapter for each type of memory card and into which each type of memory card is inserted, which provides a unique direct current voltage level on the pair of card detect lines for the single type of memory card that it accepts. Thus, I believe one of ordinary skill in the art would not find the statement that Mr. Buscaino cites to provide any meaningful discussion for interpreting the "mapping" elements of the '424 or '847 patents.

29. With respect to ¶ 29 of the Buscaino 2012 Declaration, I disagree with Mr. Buscaino's understanding that Figures 4 and 5 from the '424 and '847 patents, and Figure 5 from the '638 patent, alone or in combination, disclose an algorithm for the "mapping functions" recited in the claims identified in ¶ 14 above. Nowhere in the patent specifications or "pin mapping" tables of the '424 or '847 patents is there any disclosure of a step-by-step procedure (i.e., an algorithm) which a controller would execute to determine the assignment of signal lines to connector pins based upon which type of memory card is inserted into an adapter with a common set of contact pins used for multiple types of memory cards. As discussed above, the card detection technique of the '638 patent does not apply to the '424 and '847 patents. Based on my review of the Patents and prosecution histories for the Patents, the "pin mapping" tables that are shown in the tables in Figures 4 and 5 of the '424 patent and '847 patent, and in Figure 5 of the '638 patent, are a different type of "mapping" than what is claimed in claims 25 and 28 of the '424 patent and claim 1 of the '847 patent.

30. With respect to ¶ 30 of the Buscaino 2012 Declaration, nothing in ¶ 30 of the Buscaino 2012 Declaration speaks to the issue at hand – whether an "algorithm" is disclosed for mapping. It is my opinion that the patent specification does not contain any disclosure of a step-by-step procedure (i.e., an algorithm) which a controller would execute to determine the assignment of signal lines to connector pins based upon which type of memory card is inserted into an adapter with a common set of contact pins used for multiple types of memory card.

31. With respect to ¶ 31 of the Buscaino 2012 Declaration, I disagree with Mr. Buscaino's opinion that the '424 patent and the '847 patent disclose corresponding structure for performing the claimed "mapping functions" set forth in ¶ 14 above. Based upon my review of the Patents and the prosecution histories for the Patents, the only possible structure that could potentially perform the "mapping function" set forth in claims 25 and 28 of the '424 patent and claim 1 of the '847 patent is the controller or controller chip disclosed in the specification for those patents, but such controller or controller chip would need an algorithm to perform the claimed "mapping function." It is my opinion, as one of ordinary skill in the art at the time of the alleged inventions, that no such algorithm is disclosed in the Patents.

32. With respect to ¶ 40 of the Buscaino 2012 Declaration, other than the reference in the figures, I found no discussion within the '424 or '847 patents that mentions any role for the "MCMD" signal in an adapter. I found no discussion in the '424 or '847 patents that describes the MCMD signal as having any role in identification of cards. I found no discussion in the '424 or '847 patents that describes whether or how the controller processes the MCMD signal. Indeed, the term "MCMD" appears nowhere in the text of the '424 and '847 patent specifications except, as noted, Figures 4 and 5. I read the portions of the Patents' specifications to which Mr. Buscaino refers but I did not find any mention of a technique to identify cards. The text of these passages is identical. It reads: "Control signals for latch enables, write enable and protect, output enable, and ready handshake are among the control signals." I find no discussion in this passage that refers to any technique for identifying cards. I found no discussion in the '424 or '847 patents of any of the command signals listed in Mr. Buscaino's declaration – CMD0, ACMD1 (possibly

CMD1), CMD2 and CMD3. None of these terms appears anywhere in the Patents' disclosure, and none is mentioned as having any role in identification of card types.

33. With respect to ¶ 42 of the Buscaino 2012 Declaration, I reviewed the disclosure of the '424 and '847 patents. Neither patent refers to the use of any control signal to distinguish SD from MMC. In fact, neither patent mentions that an adapter ever distinguishes SD from MMC, or provides any algorithm or technique for doing so. In the '638 patent, the same adapter 32 is used for both MMC/SD and the card type detection has only one value LH (01) to identify a single card type – MMC/SD.

34. With respect to ¶ 43 of the Buscaino 2012 Declaration, I reviewed the disclosure of the '424 and '847 patents. Neither document mentions SD Specifications versions 1.0, 2.00, or 3.00 or mentions any technique that might be described in those documents for distinguishing SD from MMC cards.

35. With respect to ¶ 44 of the Buscaino 2012 Declaration, I reviewed the disclosure of the '424 and '847 patents and the statement from the '638 patent to which Mr. Buscaino refers. Based upon my review, the Patents' references to the "SD Group" do not describe any structure for identifying types of cards in an adapter.

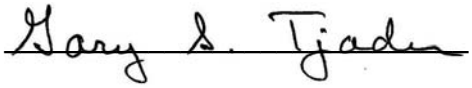
III. CONCLUSION

36. My opinions regarding Mr. Buscaino's opinions are based solely on my understanding of his opinions as articulated in the Buscaino 2012 Declaration.

37. My silence with respect to any statement from the Buscaino 2012 Declaration that is not specifically addressed above does not mean I necessarily agree with such assertion or statement, but rather that I offer no opinion on such assertion or statement at this time.

I declare that the foregoing is true and correct to the best of my information, knowledge and belief.

Dated: April 23, 2015



Gary S. Tjaden, Ph.D.

EXHIBIT 1

BIOGRAPHICAL SKETCH

Dr. GARY S. TJADEN

Education

Doctor of Philosophy, Computer Science
The Johns Hopkins University 1973

Master of Science, Electrical Engineering
Northwestern University 1969

Bachelor of Science, Electrical Engineering
University of Utah 1966

Employment History

COCOMO ID, LLC
Founder/CEO 1996-Present

Expert Witness Consulting
Consultant as expert witness in patent litigation 2000-Present

Georgia Institute of Technology
Principal Research Engineer 1993-2004

Polytechnic University
Industry Professor of Computer Science 1992-1993

NYNEX Corp.
President, NYNEX ALLINK Co. 1989-1992
Director, Information Systems & Services Lab. 1987-1989

Burroughs/Unisys Corp.
V.P. & Gen. Mgr., Third Party Programs 1985-1987
V.P. Systems Architecture 1984-1985

Cox Cable Communications
Senior V.P., Engineering & Technology 1979-1984

Sperry Corp.
Director, Hardware Tech., Univac Division 1976-1979
Member Tech. Staff, Sperry Research Center 1975-1976

Bell Telephone Labs
Member Tech. Staff, Advanced Tech. Lab. 1972-1975
Member Tech. Staff, Electronic Switching Systems Division 1966-1970

Experience Summary

Expert witness in patent infringement litigation since 2000.

Founder, President of COCOMO ID, LLC, a company that develops and markets technology for mobilized text-audio publishing. Technology based on patents awarded to founder.

During eleven years at Georgia Institute of Technology responsible for directing the activities of a Georgia Tech interdisciplinary research center, called the Center for Enterprise Systems. The mission of the Center was to help commercial enterprises to use information technology to support business strategy. Retired from Georgia Tech November, 2004.

Background of some twenty-five years of experience in the computer and communications industries. Specific activities and responsibilities include:

- Founder and general manager of NYNEX subsidiary company which develops and markets turnkey real-time decision support systems to improve the management of large heterogeneous corporate networks and distributed systems.
- Established and managed applied research laboratory responsible for development and transfer of new technologies and product concepts in the area of data communications-based information systems and services.
- Led the development and commercial production of a distributed information system based on off-the-shelf components including UNIX workstations and servers, an expert system, a relational database management system, and an object-oriented graphical user interface.
- Responsible for Burroughs' corporate third party software strategy, general management of cross-industry application software Line Of Business, and use of third party technologies to satisfy product needs in all product areas.
- Responsible for technology strategy, R&D of interactive CATV information systems, cable system design, and for construction and technical operation standards and quality control for an operator of some 60 cable television systems serving more than 1.3 million subscribers.
- Responsible for management of all advanced hardware technology activities for major supplier of mainframe computer systems. Technologies included VLSI design and fabrication, disk and optical memories, and mainframe architectures.
- Member of a 3-person team that developed a new, patented architecture for designing mainframe central processors from off-the-shelf LSI chip sets at research arm of major supplier of mainframe computer systems. Technology commercialized as Univac 1160 mainframe computer.
- Member of advanced technology development group in the Electronic Switching Systems (computer-based telephone central office switches) for AT&T Bell Laboratories. Worked on advanced operating system for telephone switching systems, and new switched services such as centralized voice-mail and e-mail.
- Member of group developing telephone switching system peripheral components. Inventor of new technology for using LSI to detect on-hook/off-hook state changes on telephone lines.

Fields of Interest

Political economy, complex adaptive systems, business process engineering, impact of information technology on business strategy, management of information technology and information systems, distributed systems architecture and management; computer communication and networking; distributed application software architectures, and distributed mobile systems.

Special Honors and Awards

Samuel N. Alexander award from Washington D.C. regional ACM chapter for outstanding student of Computer Science in 1971-72
Elected to Sigma Xi
Elected to Eta Kappa Nu
M.S. studies supported under Bell Labs Graduate Study Program
Graduated Cum Laude from U. of Utah under Honors Program
Distinguished Lecturer award from Stanford University Computer Forum

Professional Affiliations

Session Chair, IEEE International Workshop on Systems Management, April 1993
Member IEEE Computer Society 1972 - 1973
Vice Chairman of 1979 Computer Architecture Symposium
Member of Program Committee, 1978 Computer Architecture Symposium
Chairman of Panel Session on Implications of VLSI on Computer Design, 1979 ACM National Conference
Member of NSF Committee on the National Telecommunications Network, representing CATV industry, 1983
Two term Chairman of CATV trade Association Engineering Committee, 1982-84

Patents

1. "Supervisory Circuit for Telephone Lines," No. 3,622,709, assigned to Bell Labs
2. "Bus Coupler Protection Circuit," No. 3,654,517, assigned to Bell Labs
3. "Microprogrammable Computer Utilizing Concurrently Operating Processors," No. 4,199,811, assigned to Sperry Corp
4. "One's Complement Subtractive Arithmetic Unit Utilizing Two's Complement Arithmetic Circuits," No. 4,099,248, assigned to Sperry Corp
5. "Digital Computer with Overlapped Operation Utilizing Conditional Control to Minimize Time Losses," No. 4,210,960, assigned to Sperry Corp
6. "Table Driven Decision and Control Logic for Digital Computers," No. 4,237,532, assigned to Sperry Corp
7. “Personalized Audio Information Delivery System,” No. 5,915,238, assigned to Cocomo ID.
8. “Personalized Audio Information Delivery System (continuance),” No. 6,122,617, assigned to Cocomo ID.

Trials or Depositions As Expert Witness

Superguide Corp. and Gemstar Development Corp. vs. DirecTV, Thomson, and EchoStar, U.S. District Court for the Western District of North Carolina, Asheville Division. Opined on invalidity for defendants EchoStar and Thomson, and non-infringement for EchoStar.

Certain Set-Top Boxes and Components Thereof, U. S. International Trade Commission, Wash. D.C., Honorable Paul L. Luckern. Opined on invalidity for defendants Scientific Atlanta and Pioneer.

Gemstar Development Corporation MDL Patent Litigation. Opined on invalidity and non-infringement for defendant Scientific Atlanta. Deposed multiple times with respect to two groups of patents.

Finisar Corporation vs. DirecTV, U.S. District Court, Eastern District Of Texas, Beaumont Division. Opined on invalidity for defendant DirecTV.

TV Guide Online, Inc. and TV Guide Online, LLC vs. Tribune Media Services, Inc., U.S. District Court, District Of Delaware. Opined on invalidity and non-infringement for defendant Tribune Media Services.

Major Reports and Publications

1. "Measuring The Information Age Business" Technology Analysis and Strategic Management, Vol. 8, No. 3, 1996, pp. 233-246. Also published in The Information Revolution, edited by Porter, A. & Read, W., Ablex Publishing, 1998, Chapter 1.

2. "Structural Effectiveness Metrics for Business Processes," co-authored with S. Narasimhan and S. Mitra, INFORMS Conference on Information Systems and Technology, Washington, DC, May, 1996.

3. "Business Process Metrics of Effectiveness," co-authored with S. Narasimhan and S. Mitra, Third Eurpoean Academic Conference on Business Process Redesign, Cranfield University, UK, Feb. 1996.

4. "Network management under the umbrella," Networking Management 10, (9), August 1992, pp. 39-41

5. "OSF/DME as an Application Platform", Proceedings of Interop '91 Fall, San Francisco, Calif., 9-11 October, 1991

6. "The Allink Approach to Integrated Network Management," Network and Distributed Systems Management '91 Conference, Technology Transfer Institute, 18-20 September 1991, Washington D.C.

7. "Using Expert Systems for Real-Time Integrated Network Management," Communications Networks West, San Francisco, Calif., 15-18 July 1991

8. "Integrated Network Management for Real-Time Operations," IEEE Network 5, (2), March 1991, pp. 10-15, coauthor

9. "Automating Integrated Network Management," Network Management Solutions Conference, Anaheim, Calif., April 10-12, 1990

10. "Integrated Network Management for Real-Time Operations," Proceedings of NOMs '90, IEEE Coms. Society, San Diego, Calif., Feb. 11-14, 1990

11. "Switched Voice on a CATV System", Proceedings of GLOBECOM '83, November 1983

12. "The INDAX Two-Way CATV Network For Videotex Services," VideoTex – Key To The Information Revolution, (Northwood Hills, Middlesex, UK), June, 1982, pp 465-475, coauthor

13. "INDAX: An Operational Interactive Cable Television and Home Information System", Proceedings of COMPCON Spring '82, February 1982, pp 356-359, coauthor

14. "Some Considerations in the Design of Mainframe Processors with Microprocessor Technology," IEEE Computer 12, (8), August 1979, coauthor

15. "Impact of LSI Technology on Computer Architecture", Proceedings of 1979 Computer Architecture Symposium

16. "Hierarchical Properties of Concurrency," Proceedings of 1979 International Conference on Parallel Processing

17. "Non-Custom Design for NMOS VLSI," 1979 Custom Integrated Circuits Conference, U. of Rochester

18. "Mainframe Implementation With Off-the-shelf LSI Modules," IEEE Computer 11, (7), July 1978, pp. 42-48, coauthor

19. "Can Mainframe Performance Be Achieved With Microprocessor Systems?," Infotech International, 1977

20. "Applying LSI Technology to Mainframe Computers," 1977 MIDCON Conference, November 1977

21. "MIMD Multimicroprocessors as Mainframe Replacements," Workshop on Microprocessors, Northwestern University, May 1976

22. "Analysis of New Telecommunication Services Via System Attributes," Proceedings of International Communications Conference, San Francisco, June 1975, coauthor

23. "Representation of Concurrency with Ordering Matrices," IEEE Trans. On Computers", C-22, (8), August 1973, coauthor

24. "Representation and Detection of Concurrency Using Ordering Matrices," Ph.D. Dissertation, The Johns Hopkins University, September 1972

25. "Detection and Parallel Execution of Independent Instructions," IEEE Trans. On Comp., C-19, (10), October 1970, pp. 889-895, coauthor